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09/924,185	08/02/2001	Michael Holtzman	10519-335	2657

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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/924,185	HOLTZMAN ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-11,15-25,65 and 66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-11,15-25,65 and 66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20020924; 20060315*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3, 10, 11, and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over European Patent Application Publication Number 0 292 248 to Steiner et al. ("Steiner"), US Patent Number 5,544,356 to Robinson et al. ("Robinson"), and knowledge commonly known in the art, as evidenced by US Patent Number 6,088,761 to Aybay ("Aybay"), US Patent Number 6,191,663 to Hannah ("Hannah"), and US Patent Number 4,882,554 to Akaba et al. ("Akaba") and "MULTOS – a definition from Whatis.com" ("MULTOS").

3. In reference to Claims 3 and 10, Steiner discloses an add-on smart card (See Figure 1 Number 3) for detachably coupling to a processing system (See Figure 1 Number 1) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Figure 1 Number 5); a program storage memory storing at least one operating sequence (See Figure 1

Number 7); a mass storage memory including a portion for storing user data (See Figure 1 Number 9) and a program memory portion storing an additional operating sequence (See Figure 1 Number 8); a processing unit coupled to said interface, said program storage memory, and said mass storage memory (See Figure 1 Number 4), whereby the processing unit operates on user data transferred between the mass storage memory and the processing system through the interface according to an operating sequence selected by the processing system from said additional operating sequence (See Column 4 Lines 3-8), and a mass storage interface by which the mass storage memory is connected to a bus (See Figure 1). Steiner further discloses that the smart card has a variably sized memory partition for storing application programs (operating sequences), but does not explicitly disclose how many application programs are stored there (See Figure 1 Number 8 and Figure 2). Official Notice is taken that it is well known in the art to provide multiple different application programs in the memory of a smart card, as evidenced by MULTOS (See Page 1 Paragraphs 1-3). Steiner further discloses a bus system interconnecting the components of the card, but does not disclose a single bus to which the processing unit, the interface, and the program storage memory are connected. Official Notice is taken that it is well known in the art to interconnect elements of a computing system, such as processors, memories, and interfaces, using a single bus (a multidrop bus), as evidenced by Aybay (See Figure 1), Hannah (See Figures 4 and 13 and Column 2 Lines 8-18), and Akaba (See Figure 1 and Column 1 Lines 16-36). Steiner further does not explicitly disclose the mass storage interface is a non-linear interface, as in Claim 3, or that the mass storage

memory is a flash memory, as in Claim 10. However, Steiner does disclose that the mass storage memory may be E^2PROM or any other appropriate non-volatile Read/Write memory (See Column 2 Lines 21-23 and 51-54). Robinson discloses the use of a flash memory, which is a non-linearly accessed memory, in place of an E^2PROM as a mass memory device for storing multiple different operating sequences and user data (See Column 6 Lines 7-14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Steiner with multiple operating sequences, using a multidrop bus as the interconnect between elements, and using a flash memory as the mass memory, resulting in the invention of Claims 3 and 10, in order to allow several applications to reside on one smart card instead of requrings a separate smart card for each application (See Page 1 Paragraph 2 of MULTOS); to reduce the cost and complexity of the interconnect (See Column 2 Lines 8-18 of Hannah), and to reduce the cost and complexity of the processor, since fewer I/O pins are required; and because flash memories achieve much higher densities than E^2PROMs (See Column 6 Lines 32-40 of Robinson).

4. In reference to Claim 11, Steiner and Robinson disclose the limitations as applied to Claim 3 above. Steiner further discloses that the mass storage memory further includes a portion storing system data, whereby the processing unit can operate on data transferred between the card and the unit using the system data (See Figure 1 Number 7).

5. In reference to Claim 65, Steiner and Robinson disclose the limitations as applied to Claim 3 above. Steiner further discloses that said processing unit selectively operates in combination with a processor of said processing system on said user data received from the processing system (See Column 3 Lines 4-44).

6. Claims 15, 16, 25, and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner, Robinson, and knowledge commonly known in the art, as evidenced by Aybay, Hannah, and Akaba.

7. In reference to Claims 15 and 25, Steiner discloses an add-on smart card (See Figure 1 Number 3) for detachably coupling to a processing system (See Figure 1 Number 1) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Figure 1 Number 5); a program storage memory storing an operating sequence (See Figure 1 Number 8); a processing unit coupled to said interface and said program storage memory (See Figure 1 Number 4); a mass storage memory including a portion for storing user data coupled to said processing unit (See Figure 1 Number 9); whereby the processing unit operates on user data transferred between the interface and the portion of the mass storage memory for storing user data according to said operating sequence (See Column 4 Lines 3-8), when said operating sequence is enabled by said processing system (See Column 4 Lines 1-9) but does not operate on the user data when said

operating sequence is not enabled by said processing system (See Column 3 Lines 32-38), and a mass storage interface by which the mass storage memory is connected to a bus (See Figure 1). Steiner further discloses a bus system interconnecting the components of the card, but does not disclose a single bus to which the processing unit, the interface, and the program storage memory are connected. Official Notice is taken that it is well known in the art to interconnect elements of a computing system, such as processors, memories, and interfaces, using a single bus (a multidrop bus), as evidenced by Aybay (See Figure 1), Hannah (See Figures 4 and 13 and Column 2 Lines 8-18), and Akaba (See Figure 1 and Column 1 Lines 16-36). Steiner further does not explicitly disclose the mass storage interface is a non-linear interface, as in Claim 15, or that the mass storage memory is a flash memory, as in Claim 25. However, Steiner does disclose that the mass storage memory may be E^2PROM or any other appropriate non-volatile Read/Write memory (See Column 2 Lines 21-23 and 51-54). Robinson discloses the use of a flash memory, which is a non-linearly accessed memory, in place of an E^2PROM as a mass memory device for storing multiple different operating sequences and user data (See Column 6 Lines 7-14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Steiner using a multidrop bus as the interconnect between elements, and using a flash memory as the mass memory, resulting in the invention of Claims 15 and 25, in order to reduce the cost and complexity of the interconnect (See Column 2 Lines 8-18 of Hannah), and to reduce the cost and complexity of the processor, since fewer I/O pins are required; and because

flash memories achieve much higher densities than E^2PROMs (See Column 6 Lines 32-40 of Robinson).

8. In reference to Claim 16, Steiner and Robinson disclose the limitations as applied to Claim 15 above. Steiner further discloses that the mass storage memory includes a program memory portion storing at least one additional operating sequence (See Figure 1 Number 8).

9. In reference to Claim 66, Steiner and Robinson disclose the limitations as applied to Claim 3 above. Steiner further discloses that said processing unit selectively operates in combination with a processor of said processing system on said user data received from the processing system (See Column 3 Lines 4-44).

10. Claims 4, 8, 17, 19, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner, Robinson, and knowledge commonly known in the art as applied to Claims 3 and 15 above, and further in view of US Patent Number 6,409,089 to Eskicioglu ("Eskicioglu").

11. In reference to Claims 4 and 8, Steiner and Robinson disclose the limitations as applied to Claim 3 above. Steiner and Robinson do not disclose that the data transferred between the card and the processing system is continuous media, as in Claim 4, and that the at least two additional operating sequences includes a data

encryption/decryption routine, as in Claim 8. Steiner does disclose that the device is a smart card (See Column 1 Lines 12-26). Eskicioglu discloses a smart card that receives an audio/video stream, which is continuous media, and performing encryption and decryption on the received audio/video stream (See Figure 2 and Column 1 Lines 51-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Eskicioglu using the smart card of Steiner as modified by Robinson and knowledge commonly known in the art, resulting in the inventions of Claims 4 and 8, in order to allow the application programs to be downloaded, debugged, and tested before permanently fixing it to the smart card (See Column 1 Lines 27-30 and Column 4 Lines 12-21 of Steiner), which thus reduces development and production costs.

12. In reference to Claims 17 and 23, Steiner and Robinson disclose the limitations as applied to Claim 15 above. Steiner and Robinson do not disclose that the data transferred between the card and the processing system is continuous media, as in Claim 17, and that said operating sequence is a data encryption/decryption routine, as in Claim 23. Steiner does disclose that the device is a smart card (See Column 1 Lines 12-26). Eskicioglu discloses a smart card that receives an audio/video stream, which is continuous media, and performing encryption and decryption on the received audio/video stream (See Figure 2 and Column 1 Lines 51-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Eskicioglu using the smart card of Steiner as modified by Robinson and knowledge commonly known in the art, resulting in the inventions of Claims 17 and 23, in order to allow the application programs to be downloaded, debugged, and tested before permanently fixing it to the smart card (See Column 1 Lines 27-30 and Column 4 Lines 12-21 of Steiner), which thus reduces development and production costs.

13. In reference to Claim 19, Steiner, Robinson, and Eskicioglu disclose the limitations as applied to Claim 17 above. Steiner further discloses that a portion of the mass storage memory contains data prerecorded by the card supplier (See Column 4 Lines 1-21).

14. Claims 5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner, Robinson, knowledge commonly known in the art, and Eskicioglu as applied to Claims 4 and 17 above, and further in view of US Patent Number 5,418,752 to Harari et al. ("Harari").

15. In reference to Claim 5, Steiner, Robinson, and Eskicioglu disclose the limitations as applied to Claim 4 above. Steiner, Robinson, and Eskicioglu do not disclose a data cache memory connected to the processor and the mass storage memory for buffering the continuous media transferred between the card and the processing system. Harari

discloses the use of a data cache memory for buffering data to be transferred to a flash memory (See Abstract and Column 2 Lines 44-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Eskicioglu, as modified by Steiner, Robinson, and knowledge commonly known in the art, with the data cache buffer of Harari, resulting in the invention of Claim 5, in order to minimize the number of writes to the flash memory, and thus retard its aging by subjecting it to fewer stress inducing write/erase cycles (See Column 2 Lines 44-48 of Harari); and to increase the write throughput (See Column 2 Lines 54-56 of Harari).

16. In reference to Claim 18, Steiner, Robinson, and Eskicioglu disclose the limitations as applied to Claim 4 above. Steiner, Robinson, and Eskicioglu do not disclose a data cache memory connected to the processor and the mass storage memory for buffering the continuous media transferred between the card and the processing system. Harari discloses the use of a data cache memory for buffering data to be transferred to a flash memory (See Abstract and Column 2 Lines 44-56). Robinson discloses the use of a flash memory, which is a non-linearly accessed memory, and thus the transferred data is stored non-linearly (See Column 6 Lines 7-14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Eskicioglu, as modified by Steiner, Robinson, and knowledge commonly known in the art, with the data cache buffer of

Harari, resulting in the invention of Claim 18, in order to minimize the number of writes to the flash memory, and thus retard its aging by subjecting it to fewer stress inducing write/erase cycles (See Column 2 Lines 44-48 of Harari); and to increase the write throughput (See Column 2 Lines 54-56 of Harari).

17. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner, Robinson, and knowledge commonly known in the art as applied to Claim 3 and above, and further in view of US Patent Number 6,266,671 to Niimura ("Niimura").

18. In reference to Claims 6 and 7, Steiner and Robinson disclose the limitations as applied to Claim 3 above. Steiner and Robinson do not disclose that said at least two operating sequences includes a decompression program, as in Claim 6, or a compression program, as in Claim 7. Niimura discloses a card device having a memory which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Steiner, as modified by Robinson and knowledge commonly known in the art, with the data compression and decompression ability of Niimura, resulting in the invention of Claims 6 and 7, in order to increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

19. Claims 9 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner, Robinson, and knowledge commonly known in the art as applied to Claims 3 and 15 above, and further in view of US Patent Number 5,987,155 to Dunn et al. ("Dunn").

20. In reference to Claim 9, Steiner and Robinson disclose the limitations as applied to Claim 3 above. Steiner and Robinson do not disclose that at least two additional operating sequences includes a voice-recognition program. Dunn discloses a smart card which receives voice recognition information from the host for processing (See Column 6 Lines 8-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the voice-recognition smart card of Dunn using the smart card of Steiner as modified by Robinson and knowledge commonly known in the art, resulting in the invention of Claim 9, in order to allow the application programs to be downloaded, debugged, and tested before permanently fixing it to the smart card (See Column 1 Lines 27-30 and Column 4 Lines 12-21 of Steiner), which thus reduces development and production costs.

21. In reference to Claim 24, Steiner and Robinson disclose the limitations as applied to Claim 15 above. Steiner and Robinson do not disclose that said operating sequence

is a voice-recognition program. Dunn discloses a smart card which receives voice recognition information from the host for processing (See Column 6 Lines 8-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the voice-recognition smart card of Dunn using the smart card of Steiner as modified by Robinson and knowledge commonly known in the art, resulting in the invention of Claim 24, in order to allow the application programs to be downloaded, debugged, and tested before permanently fixing it to the smart card (See Column 1 Lines 27-30 and Column 4 Lines 12-21 of Steiner), which thus reduces development and production costs.

22. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner, Robinson, knowledge commonly known in the art, and Eskicioglu, as applied to Claim 17 and above, and further in view of Niimura.

23. In reference to Claims 20 and 21, Steiner, Robinson, and Eskicioglu disclose the limitations as applied to Claim 17 above. Steiner, Robinson, and Eskicioglu do not disclose that said operating sequence is a decompression program, as in Claim 20, or a compression program, as in Claim 21. Niimura discloses a card device having a memory which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Eskicioglu, as modified by Steiner, Robinson, and knowledge commonly known in the art, with the data compression and decompression ability of Niimura, resulting in the invention of Claims 20 and 21, in order to increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

24. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner, Robinson, and knowledge commonly known in the art as applied to Claim 15 above, and further in view of US Patent Number 5,995,018 to Hane et al. ("Hane").

25. In reference to Claim 22, Steiner and Robinson disclose the limitations as applied to Claim 15 above. Steiner and Robinson do not disclose that the data transferred between the interface and the mass storage memory is a navigation database. Hane discloses a smart card for receiving, storing, and transmitting a navigation database (See Column 8 Lines 35-44).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the smart card having a navigation database of Hane using the smart card of Steiner as modified by Robinson and knowledge commonly known in the art, resulting in the invention of Claim 22, in order to allow the application programs to be downloaded, debugged, and tested before permanently fixing it to the

smart card (See Column 1 Lines 27-30 and Column 4 Lines 12-21 of Steiner), which thus reduces development and production costs.

26. Claims 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over 2002/0195493 to Dell ("Dell") and Robinson.

27. In reference to Claims 3 and 10, Dell discloses an add-on card (See Figure 1 Number 10) for detachably coupling to a processing system (See Paragraph 15) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Figure 1 Number 14 and Paragraph 15); a program storage memory storing at least one operating sequence (See Figure 1 Number 26); a mass storage memory including a portion for storing user data (See Figure 1 Number 32) and a program memory portion storing at least two additional operating sequences (See Figure 1 Number 30 and Paragraph 19); a processing unit coupled to said interface, said program storage memory, and said mass storage memory (See Figure 1 Number 18), whereby the processing unit can operate on user data transferred between the mass storage memory and the processing system through the interface according to an operating sequence selected by the processing system from said at least two additional operating sequences (See Figure 4 and Paragraph 30); a card bus to which the processing unit, the interface and the program storage memory are connected (See Figure 1 Number 22); and a mass storage interface by which the mass storage memory is connected to the card bus (See Figure 1

Numbers 20 and 22). Dell does not disclose that the mass storage interface is a non-linear interface, as in Claim 3, and that the mass storage memory is a flash memory, as in Claim 10. Dell does disclose that the mass storage may contain ROM, RAM, and non-volatile memory (See Paragraph 18). Robinson discloses the use of a flash memory, which is a non-linearly accessed non-volatile memory, as a mass memory device for storing multiple different operating sequences and user data (See Column 6 Lines 7-14).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to construct the device of Dell with a flash memory, resulting in the inventions of Claims 3 and 10, because flash memories are notoriously old and well known and provide fast erasure and reprogramming (See Column 3 Lines 58-61 of Robinson) and provide high densities through the use of single transistor cells (See Column 6 Lines 32-40 of Robinson).

28. In reference to Claims 15 and 25, Dell discloses an add-on card (See Figure 1 Number 10) for detachably coupling to a processing system (See Paragraph 15) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Figure 1 Number 14 and Paragraph 15); a program storage memory storing an operating sequence (See Figure 1 Number 30 and Paragraph 19); a processing unit coupled to said interface and said program storage memory (See Figure 1 Number 18); a mass storage memory including a portion for storing user data coupled to said processing unit (See Figure 1 Number

32), whereby the processing unit operates on user data transferred between the interface and the portion of the mass storage memory for storing user data according to said operating sequence when said operating sequence is enabled by said processing system but does not operate on the user data when said operating sequence is not enabled by said processing system (See Figure 4 and Paragraph 30); a card bus to which the processing unit, the interface and the program storage memory are connected (See Figure 1 Number 22); and a mass storage interface by which the mass storage memory is connected to the card bus (See Figure 1 Numbers 20 and 22). Dell does not disclose that the mass storage interface is a non-linear interface, as in Claim 15, and that the mass storage memory is a flash memory, as in Claim 25. Dell does disclose that the mass storage may contain ROM, RAM, and non-volatile memory (See Paragraph 18). Robinson discloses the use of a flash memory, which is a non-linearly accessed non-volatile memory, as a mass memory device for storing multiple different operating sequences and user data (See Column 6 Lines 7-14).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to construct the device of Dell with a flash memory, resulting in the inventions of Claims 15 and 25, because flash memories are notoriously old and well known and provide fast erasure and reprogramming (See Column 3 Lines 58-61 of Robinson) and provide high densities through the use of single transistor cells (See Column 6 Lines 32-40 of Robinson).

29. In reference to Claim 16, Dell and Robinson discloses the limitations as applied to Claim 15 above. Dell further discloses that the mass storage memory further includes a program memory portion storing at least one additional operating sequence (See Figure 1 Number 30).

30. In reference to Claim 65, Dell and Robinson discloses the limitations as applied to Claim 3 above. Dell further discloses that the processing unit selectively operates in combination with a processor of said processing system on said user data received from the processing system (See Figure 4 and Paragraph 30).

31. In reference to Claim 66, Dell and Robinson discloses the limitations as applied to Claim 15 above. Dell further discloses that the processing unit selectively operates in combination with a processor of said processing system on said user data received from the processing system (See Figure 4 and Paragraph 30).

Claim Objections

32. Claim 66 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 15, from which Claim 66 depends, recites the limitations of "...the processing unit operates on user

data transferred between the interface and...the mass storage memory...according to said operating sequence when said operating sequence is enabled by said processing system but does not operate on the user data when said operating sequence is not enabled by said processing system. As the processor of the processing system determines whether or not the operating sequence is enabled, the processing unit operates in combination with the processor of the processing system. As determination is made as to whether or not to operate on the data, the processing unit is selectively operating. Thus, the limitations of Claim 66 do not further limit Claim 15.

Information Disclosure Statement

33. The information disclosure statements (IDS) submitted on 24 September 2002 and 15 March 2005 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the Examiner.

Response to Arguments

34. Applicant's arguments filed 16 July 2007 with regards to Claims 15-25 have been fully considered but they are not persuasive.

35. Applicant's arguments with respect to Claims 3-11 and 65-66 have been considered but are moot in view of the new ground(s) of rejection.

36. Applicant did not traverse the Examiner's assertion of Official Notice in the previous Office Action. As such, the common knowledge and well-known in the art statements of the previous Office Action, that it is well known in the art to interconnect elements of a computing system, such as processors, memories, and interfaces, using a single bus (a multidrop bus), are taken to be admitted prior art because of Applicant's failure to traverse the Examiner's assertion of Official Notice (MPEP 2144.03 (C)).

37. Applicant has argued that Steiner does not disclose operating on user data according to an operating sequence when the operating sequence is enabled by the processing system and not operating on the user data when the operating sequence is not enabled by the processing system (see Page 9 Section B). In response, the Examiner notes that, as shown in the above rejections, when the processing system wished to perform normal communications with the card, it enables the application program (operating sequence); and when the processing system wishes to load a new application program on the card, the current application program is erased, and thus, disabled (See Column 3 Lines 32-38 and Column 4 Lines 1-9). Thus, the data is operated on by the application program when it is enabled, and is not operated on by the application program when it is disabled.

Conclusion

38. The following prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: US Patent Number 5,530,232 to Taylor, US Patent Application Publication Number 2002/0125328 to Sukeda et al., US Patent Application Publication Number 2002/0066792 to Guthery et al., US Patent Application Publication Number 2001/0006195 to Sukeda et al., US Patent number 6,961,587 to Vilppula et al., and US Patnet Number 6,590,464 to Oda, which disclose that it is well known in the art to store multiple application programs on a smart card.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
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